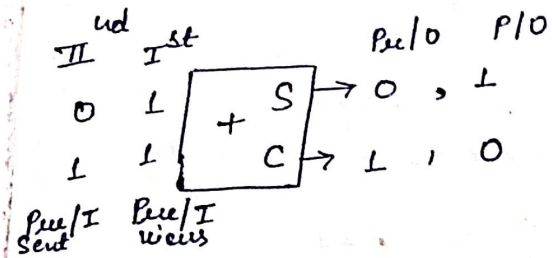
Introduction To Sequential Circuits

→ These are the combinational circuits with memory

→ In Sequential circuits, the Present O/P depends on the present I/P as well as Previous O/P.



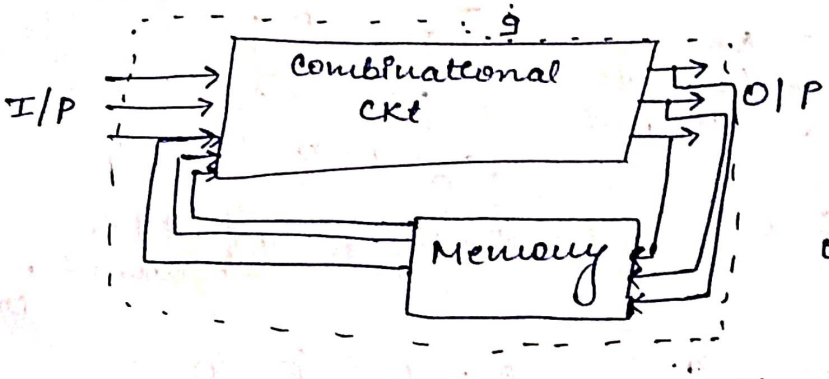
Counter :-

0 → 9

0 → +1
1 → +1
2 → +1
3 → +1
4 → +1
5
9

Flip Flop Counter Register

(Previous O/P → Store)

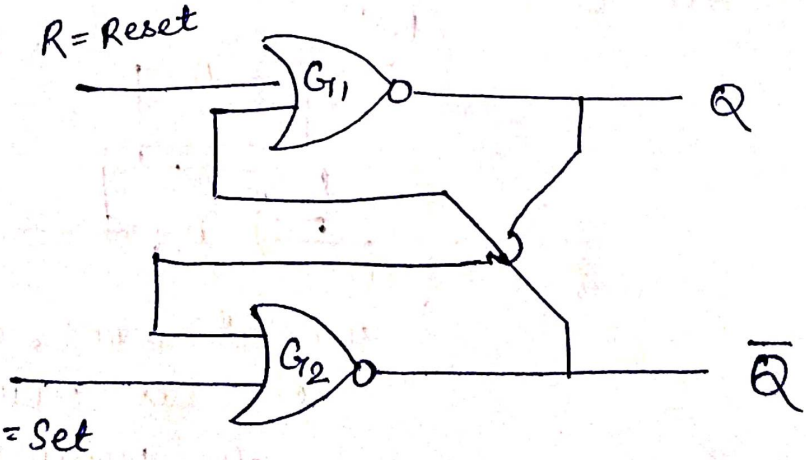


Sequential circuit

0, 1 → Store in memory. Only store 1 bit either 0 or 1 → Flip Flop → Latch

SR LATCH Using NOR Gate :-

↳ The basic storage Element is called LATCH.



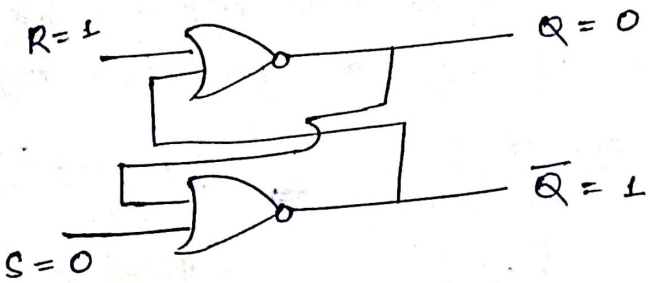
Reset = Q = 0, R=1

Set = Q = 1, S=1

NOR Gate :-

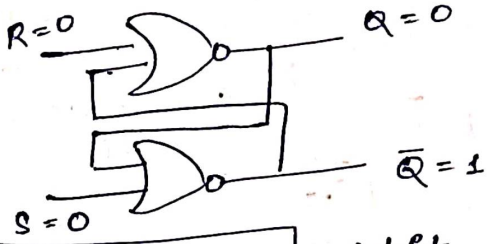
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Case-1 $S = 0$ $Q = 0$
$R = 1$ $\bar{Q} = 1$



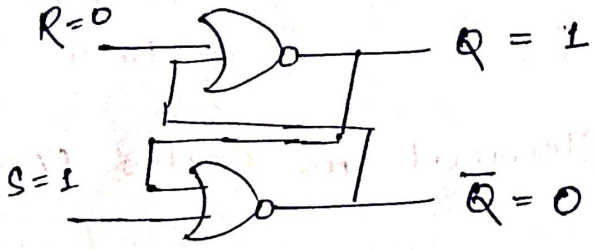
we check this process in store in memory or not ?

$S = 0$, $R = 0$ } Remove both the input



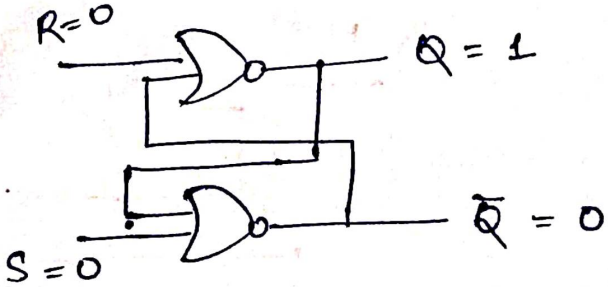
$S = 0$, $R = 0$, $Q = 0$, $\bar{Q} = 1$ → 1 bit stored in the latch.

Case-II nd :- $S = 1$ $Q = 1$ $\bar{Q} = 0$
$R = 0$



when both the input are 0

↳ $S = 0$, $Q = 1$
$R = 0$ $\bar{Q} = 0$

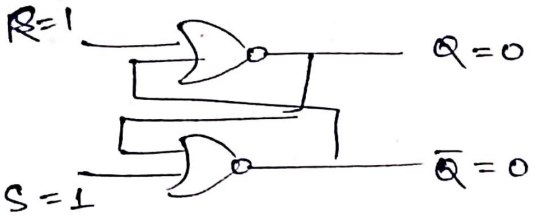


this is work as memory. one bit store in memory.

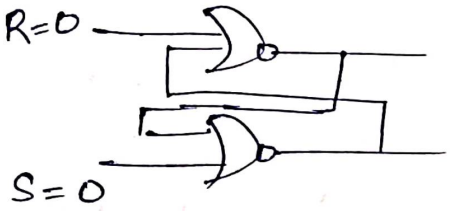
Case - III rd

S = 1 , R = 1 Q = 0 $\bar{Q}$ = 0

NOT True Becoz both are complementary.



S = 0 Q =
R = 0 $\bar{Q}$ =



I st, II nd S = 0
R = 0

Q = 0 ; Q = 1
$\bar{Q}$ = 1 $\bar{Q}$ = 0

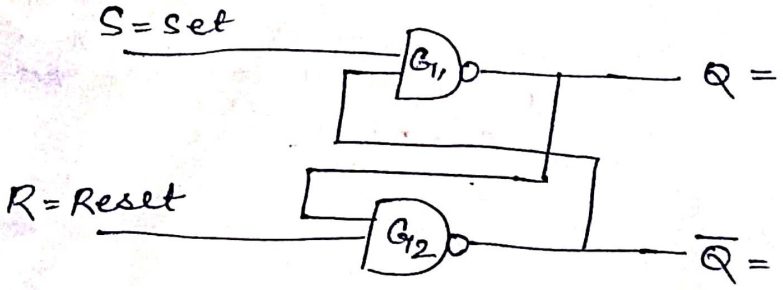
I st, II nd

This is contradictory state. In this S = 1, R = 1 never used.

Truth Table For SR Latch :-

S	R	Q	$\bar{Q}$	
0	0	Previous State (Memory)		
0	1	0	1	Reset
1	0	1	0	Set
1	1	Not used.		

SR LATCH USING NAND GATE :-



Truth Table of NAND

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Set = Q = 1
Reset = Q = 0

Case-1st S = 0, R = 0 → Q = 1, $\overline{Q}$ = 1 } NOT True

NOT USED THIS STATE

Case-2nd S = 1, R = 0 → Q = 0, $\overline{Q}$ = 1

Case-3rd S = 0, R = 1 → Q = 1, $\overline{Q}$ = 0

S = 1, R = 1 Previous state store

Case-4th S = 1, R = 1 → Q = Previous state, $\overline{Q}$ = Previous state

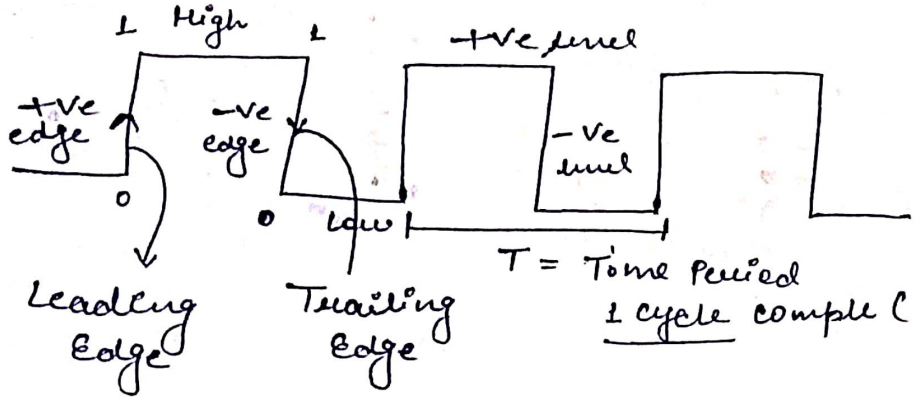
S = 1, R = 1 Previous state store

Truth Table SR LATCH USING NAND GATE :-

S	R	Q	$\overline{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	Previous State	

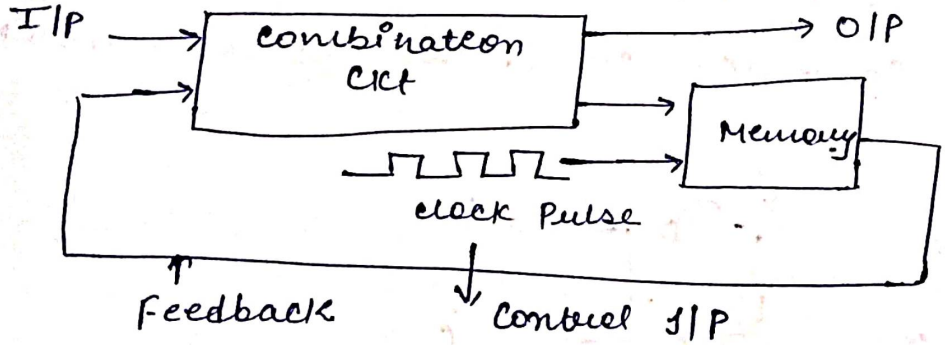
Clock & Triggering Methods

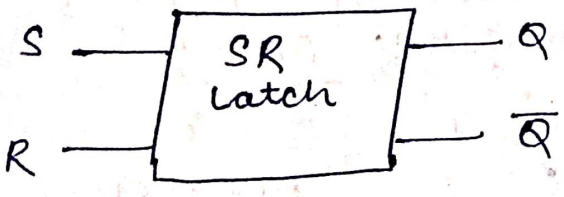
→ Clock Signal is a Timing Signal.
→ It is used to Provide Sequence of the ckt.
→ Clock is a rectangular Signal called clock Pulse with duty cycle equal to 50%.



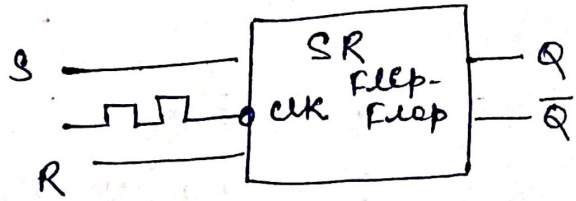
Clock Frequency = $\frac{1}{T}$

1 cycle comple (High + low)

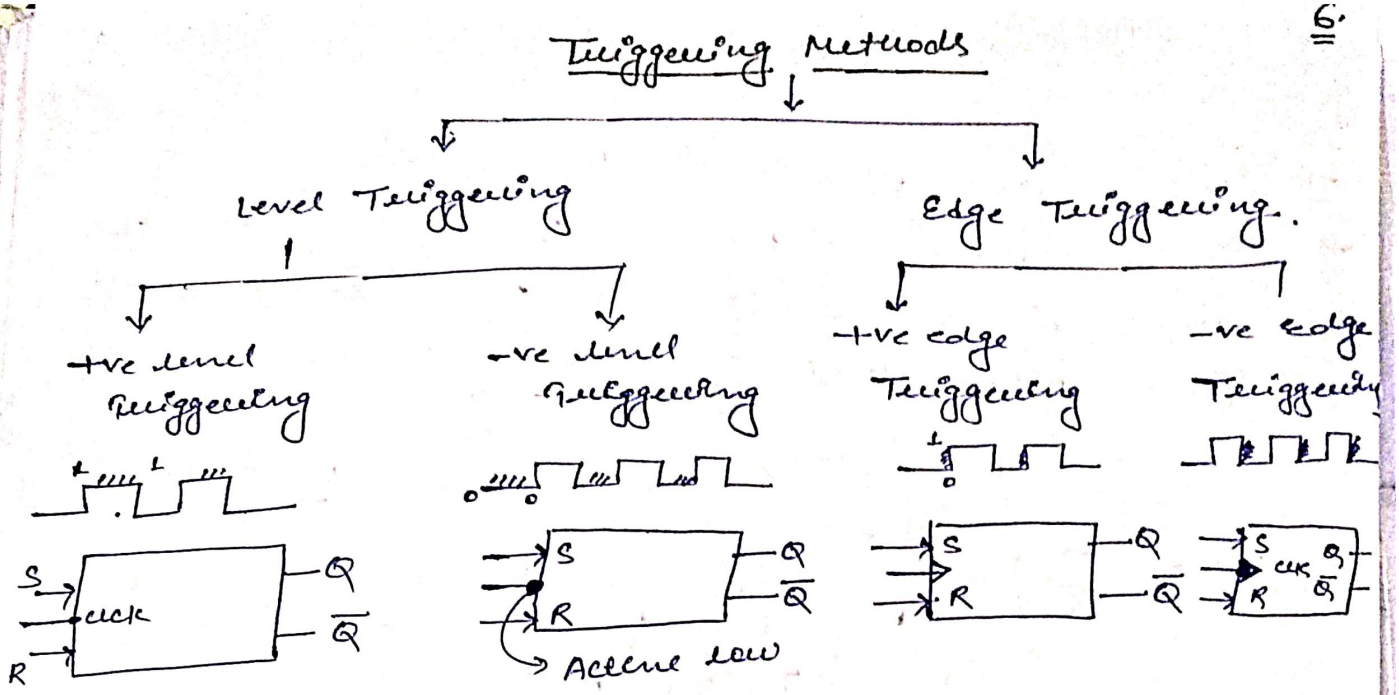




Latch behaves like Asynchronous becoz latches change the i/p & it effects the O/Ps.
If any noise / Hazards are there due to this O/P may vary.



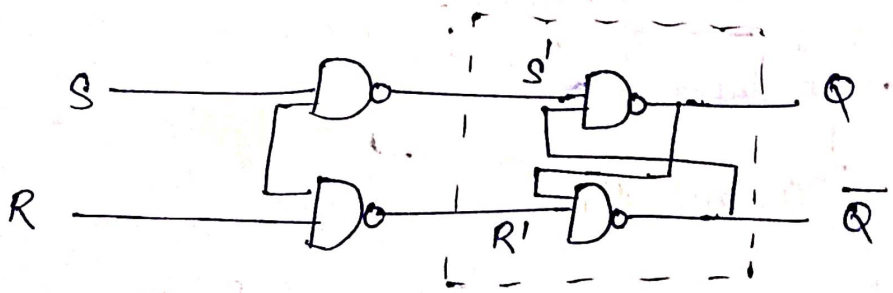
→ Behave like Synchronous ckt & use like Sequential ckt.
→ when change in the i/p then clk Pulse decide that O/P change or not.



SR flip flop :- SET RESET FLIP-FLOP

→ we can using both latch & flip flop to store one bit of memory element.

→ flip-flop is Sequential ckt & use synchronous ckt.



$S' = \overline{S.CLK}$

$S' = \overline{S} + \overline{CLK}$ — (1)

$R' = \overline{R.CLK}$

$\overline{R} + \overline{CLK}$ — (2)

Truth Table of SR latch with NAND Gate :-

S'	R'	Q	$\overline{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	Prev. State (Memory)	

CLK = 0

$S' = \overline{S} + 1 = 1$ (0 or 1)

$R' = \overline{R} + 1 = 1$ (0 or 1)

II nd case CLK = 1

$S' = \overline{S} \cdot 0 = \overline{S}$

$R' = \overline{R} \cdot 0 = \overline{R}$

I) $S' = \overline{S}$, $R' = \overline{R}$] I) $S = 0, R = 0$ / $S' = 1, R = 1$

II) $S = 0, R = 1$
$S' = 1, \overline{R} = 0$

III) $S = 1, R = 0$
$S' = 0 \quad R' = 1$

(IV) $S = 1, R = 1$
$S' = 0, R' = 0$

Clock :- CLK = 0
CLK = 1

Truth Table of SR FF

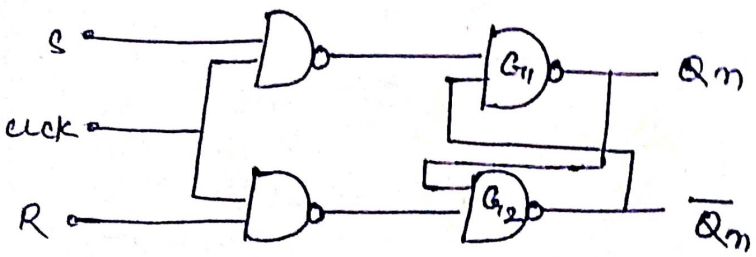
CLK	S	R	Q	$\overline{Q}$
0	x	x	Pre state Memory.	
1	0	0	Pres state	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used. (Invaled O/P)	

NAND Gate

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Characteristic Equation for SR FF :-

When we convert a FF to another FF then we need to this Equ^n.



Present state = Qn

Next State = Qn+1

Truth Table for SR FF

CLK	S	R	Q_{n+1}	
0	x	x	Q_n	
1	0	0	Q_n	
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Invalid	

Characteristic Table :-

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	(x) don't care (d)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	d (x) - don't care

Q_n \ R_nS_n	00	01	11	10
0	0	0	X	1
1	1	0	X	1

$$Q_{n+1} = R_n + Q_n\bar{S}_n$$

Characteristic equation for SR FF.

Excitation Table For SR FF :-

When we design a counter then we need to this excitation Table For SR FF.

Present State	Next State	I/P	
Q_n	Q_{n+1}	S_n	R_n
0	0	0	0 / 1 (x = don't care)
0	1	1	0
1	0	0	1
1	1	x (1 / 0)	0

Char. Table

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

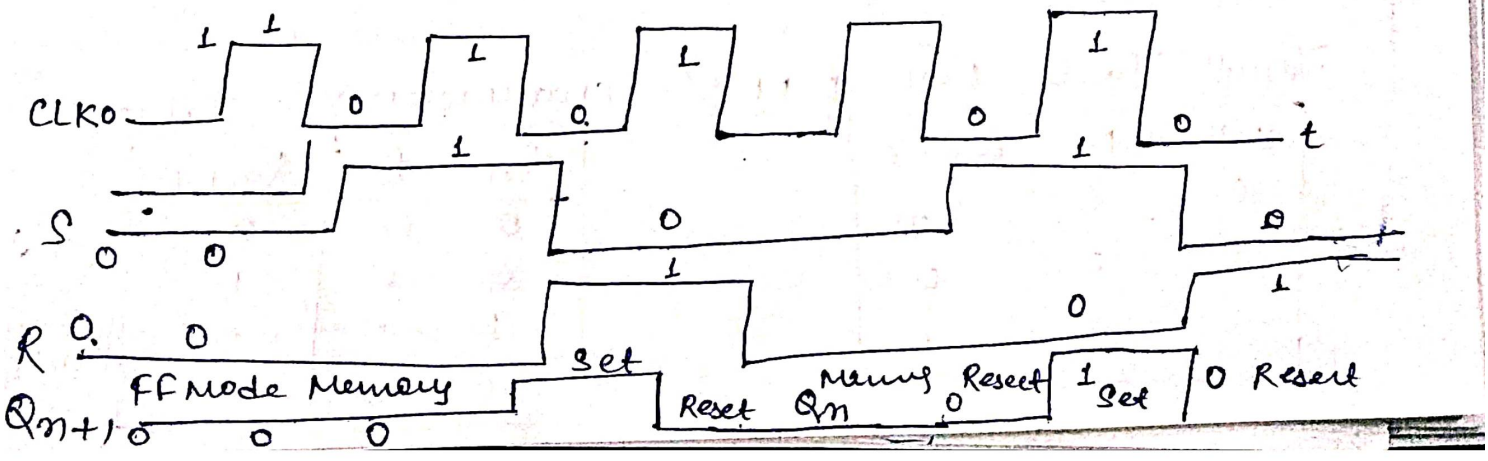
Timing Diagram For SR FF :-

Truth Table For SR FF

CLK	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	invalid

Truth Table

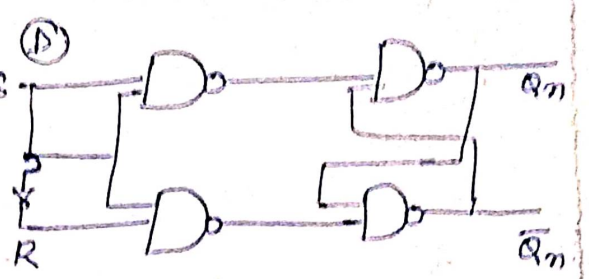
S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?



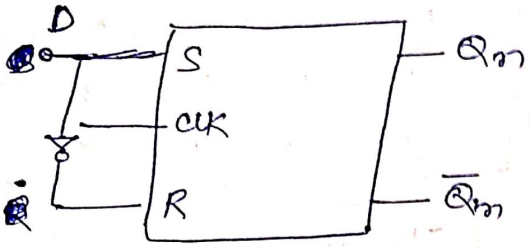
D Flip Flop

Truth Table of SR FF :-

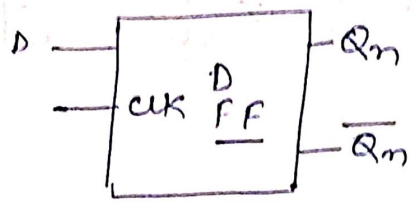
CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0 → Reset
1	1	0	1 → Set
1	1	1	Invalid



S = 1, R = 0 Q_n = 1 set
S = 0, R = 1 Q_n = 0 Reset



OR



CLK	D	$\overline{Q_{n+1}}$
0	X	Q_n
1	0	0
1	1	1

When clock pulse 0 then it store the data of previous state. (Memory) when we change the clock pulse 1 then it change the o/p accordingly.

→ D flip flop is known as "Data flip flop".

Characteristic Equation & Excitation Table for D-FF :-

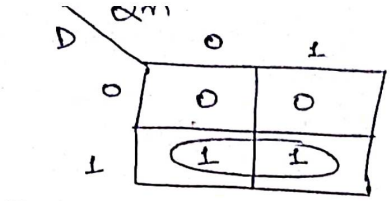
Truth Table for D FF :-

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Characteristic Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

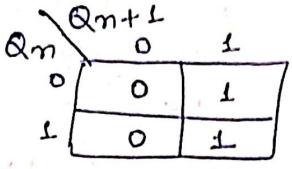
$Q_{n+1} = D$



$Q_{n+1} = D$

Excitation Table :- This Table is used for counter to find present or previous state O/P. & Find input of the FF used.

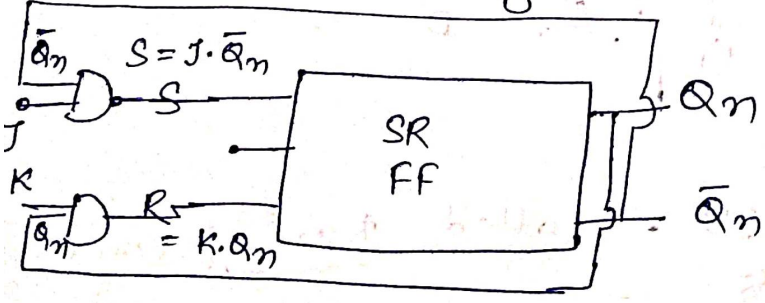
Present State	Next State	i/p
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1



$Q_{n+1} = D$

JK Flip-Flop

The JK FF is basically a gated SR FF with the addition of a clock input circuitry that prevents the illegal or invalid O/P conditions that can occur when both i/p S & R are equal to logic level '1'.



CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

J	K	Q_n	$\overline{Q_n}$	$S = J \cdot \overline{Q_n}$	$R = K \cdot Q_n$	Q_{n+1}	
0	0	0	1	0	0	0	Q_n
0	0	1	0	0	0	1	
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	
1	1	0	1	1	0	1	$\overline{Q_n}$
1	1	1	0	0	1	0	

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Assume :-

1) $Q_n = 1$ 2) $Q_n = 0$
$\overline{Q_n} = 0$ $\overline{Q_n} = 1$

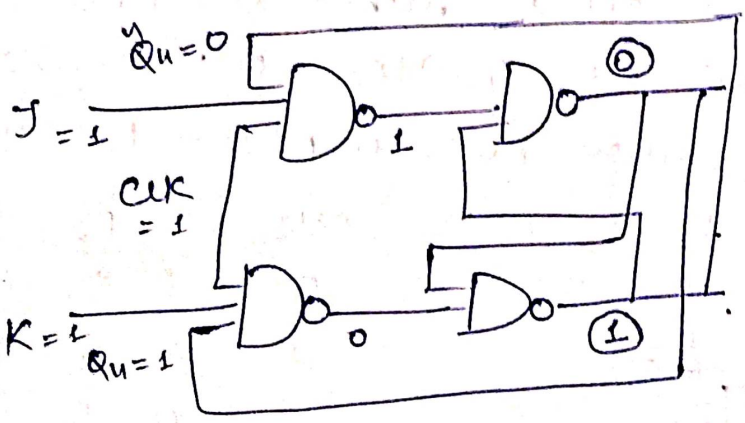
get opposite in both the cases.

& if we feed again then again O/P change → Racing b/w 0 & 1, complement of

J = 1 O/P.

K = 1

wrong.



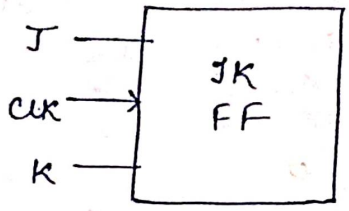
$\overline{Q_n}$ → Not predictable → called Racing condition

13.

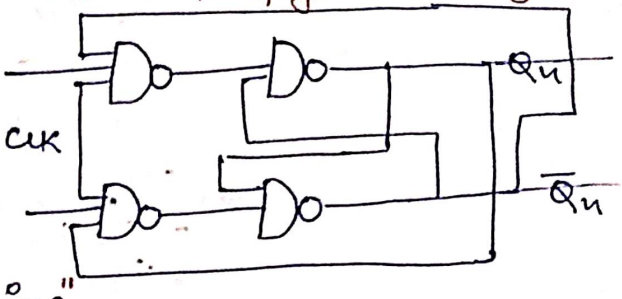
Race Around Condition

Truth Table For JK FF :-

Clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q}_n$



I/P → Propagation Delay → O/P

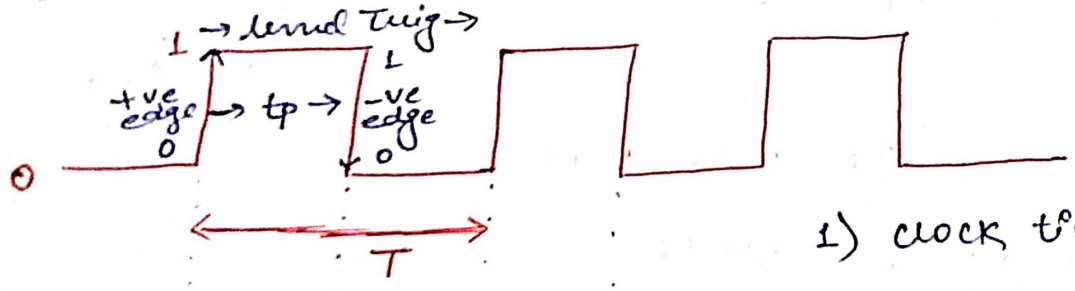


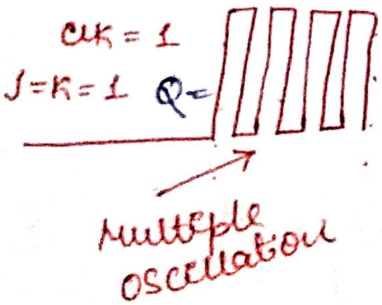
Clk = 1 , J = 1 , K = 1

$\overline{Q}_n$ = 1, 0, 1, 0 . . .

Q_n = 0, 1, 0, 1 . . .

This is called "Racing".





1) Clock time

tp < Propagation Delay.

→ Nanoseconds only.

2) Edge Triggering

→ +ve Edge Trigg.

→ -ve Edge Trigg.

↳ Master Slave JK FF

Characteristic Equation & Excitation Table For JK FF

Truth Table For JK FF

Clk	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

Characteristic Table For JK FF

Q_n	J	K	Q_{n+1}
0	0	0	$0 = Q_n$
0	0	1	0
0	1	0	1
0	1	1	$\overline{Q_n} = 1$
1	0	0	$Q_n = 1$
1	0	1	0
1	0	0	1
1	1	1	$\overline{Q_n} = 0$

Excitation Table For JK FF

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_n \ Q_{n+1}	0	1
0	0	1
1	X	X

$J = Q_{n+1}$

Q_n \ Q_{n+1}	0	1
0	X	X
1	1	0

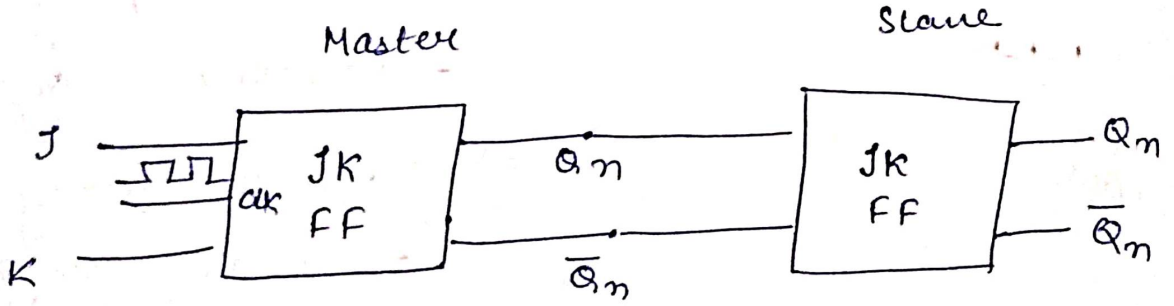
$K = \overline{Q_{n+1}}$

Q_n \ JK	00	01	11	10
0	0	0	(1)	(1)
1	(1)	0	0	(1)

$Q_{n+1} = \overline{Q_n} J + Q_n \overline{K}$

Master - Slave JK Flip - Flop :-

→ One FF is - Master
another is slave.



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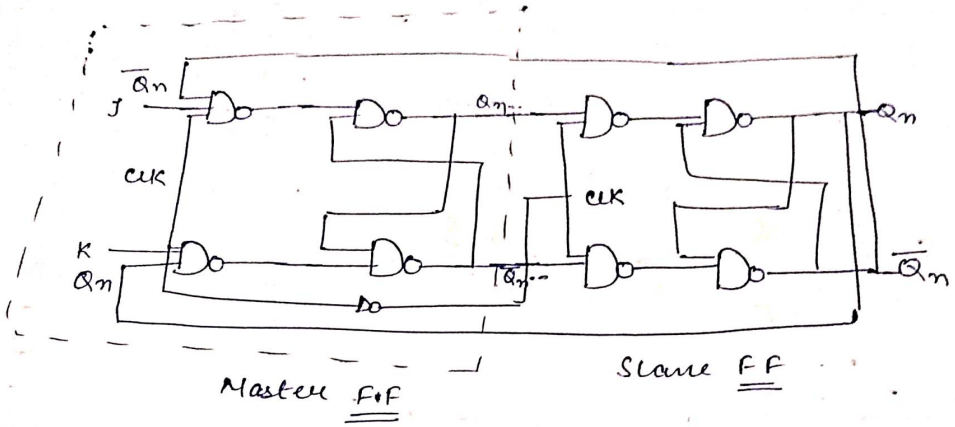
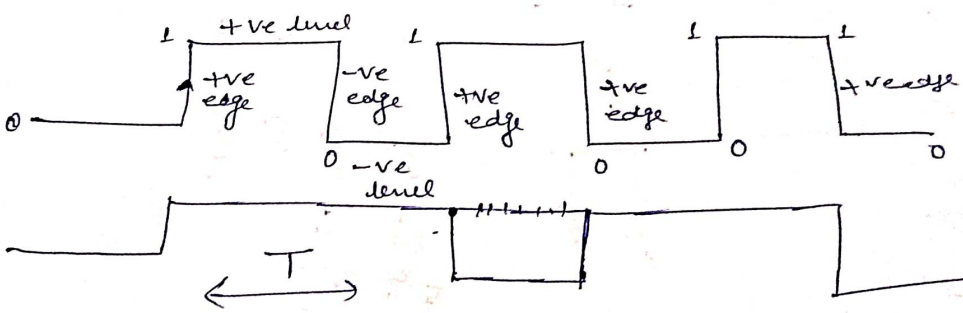
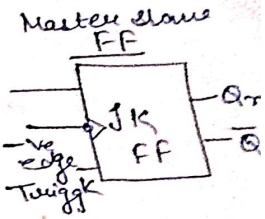


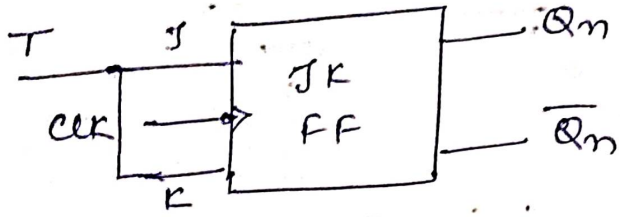




CLK = 1, J = 1, K = 1, Q_n = Toggling

Toggle FF :- T FF
↳ This is for Toggling the I/P.

→ We are using JK flip flop for T FF.



clk	J	K	Qn+1
0	X	X	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

clk	T	Qn+1	
0	X	Qn	
1	0	Qn	→ J=0, K=0
1	1	$\overline{Q_n}$	→ J=1, K=1

Characteristic Table of T FF :-

Q_n	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

Qn \ T	0	1
0	0	1
1	1	0

$Q_{n+1} = Q_n\overline{T} + \overline{Q_n}T$

$Q_{n+1} \rightarrow Q_n \oplus T$

Excitation Table of T FF :-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

FLIP FLOP CONVERSION

→ JK flipflo T flip flop :-

Step - 1 Identify available & Required FF

Available → JK FF

Required → T FF

Step - 2 Make excitation table for Available FF.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step - 3 Make characteristic table for Required FF

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step-4 Write Boolean Expression for 18. available FF.

Q_n	T	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

For J =

Q_n \ T	0	1
0	0	1
1	X	X

$J = T$

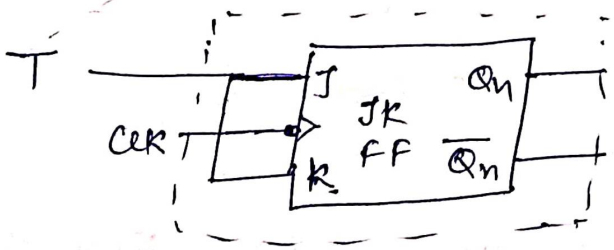
For K =

Q_n \ T	0	1
0	X	X
1	0	1

$K = T$

$$\boxed{J = K = T}$$

Step-5. Draw the circuit diagram :—



T FF

2. JK FF to D FF :-

1) Identify available & Required FF.
2) Make available - Excitation table for available FF.
3) Make characteristic table for required FF.
4) Write Boolean Expression for the available FF.
5) Draw the CKt diagram..

→ (1) Available – JK
Required = D

→ (2) Excitation Table for JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

→ (3) Characteristic Table for D

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

4. Basically we Extend the characteristics Table for Boolean Expression

Q_n	D	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

For J =

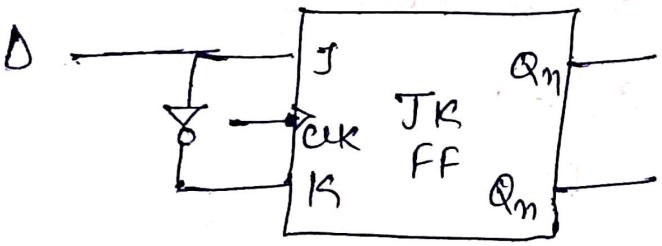
Q_n \ D	0	1
0	0	1
1	X	X

$J = D$

For K =

Q_n \ D	0	1
0	X	X
1	1	0

$K = \overline{D}$



D flip flop

JK FF to SR FF :-

Step-1 Available FF = JK
Required FF = SR

Step-2 Excitation Table for Available FF.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Characteristic Table for Required FF

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Invalid (X)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Invalid (X)

Step-4 Boolean expression for Available FF.

	Q_n	S	R	Q_{n+1}	J	K
	0	0	0	0	0	X
	0	0	1	0	0	X
	0	1	0	1	1	X
Not used	0	1	1	Invalid (X)		
	1	0	0	1	X	0
	1	0	1	0	X	1
Not used	1	1	0	1	X	0
	1	1	1	Invalid (X)		

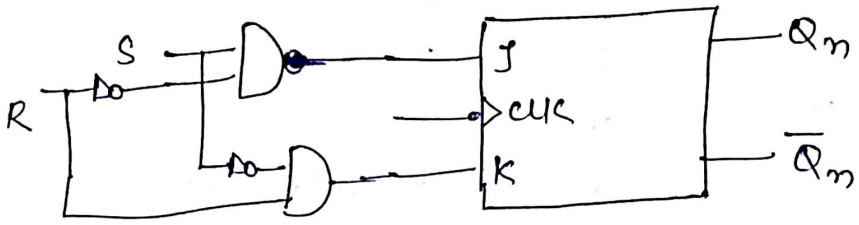
Q_n \ SR	00	01	11	10
0	0	0		1
1	X	X		X

$Q_{n+1} = J = S\bar{R}$

Q_n \ SR	00	01	11	10
0	X	X		X
1	0	1		0

$K = \bar{S}R$

Step-5 Draw the circuit diagram :-



JK to SR flip-flop

SR FF to JK FF :-

1) Available = SR
Required = JK

2) Excitation Table → SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3) Characteristic table for → JK

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

S

4) Boolean Expression for SR.

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

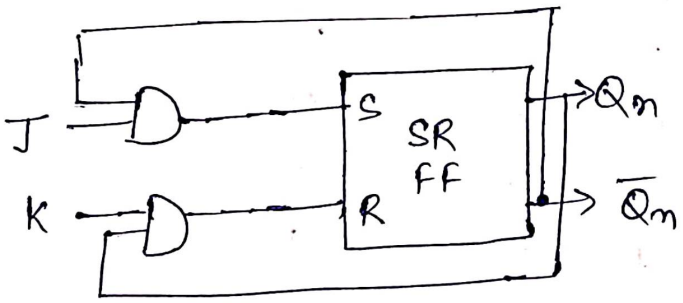
Q_n \ JK	00	01	11	10
0	0	0	1	1
1	x	0	0	x

For $S = \overline{Q}_n J$

Q_n \ JK	00	01	11	10
0	x	x	0	0
1	0	1	1	0

For $R = Q_n K$

Step-5 Draw the circuit Diagram for this :-



SR to JK flip flop

SR FF To T FF :-

Step-1 ≡ Available FF → SR
Required FF → T

Step-2 ≡ Excitation Table → SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step-3 ≡ Characteristic table for - T

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step-4 ≡ Boolean Expression for SR

Q_n	T	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	0	1
1	1	0	X	0

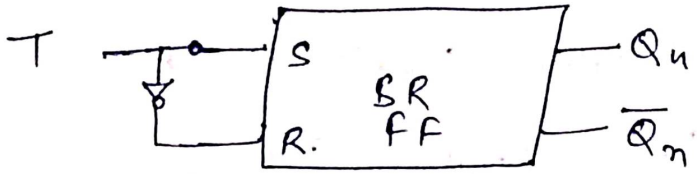
Q_n \ T	0	1
0	0	1
1	0	X

$S = T$

Q_n \ T	0	1
0	X	0
1	1	0

$R = \overline{T}$

Step-5 :- Draw the circuit diagram for this.



SR FF To T FF

SR to D FF :-

1) Available - SR
Required → D

2) Excitation → SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3) Characteristic - D

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Boolean expression for SR :-

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

S	R
0	X
1	0
0	1
X	0

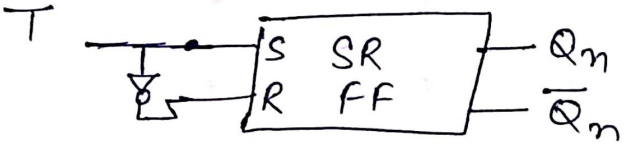
Q_n \ T	0	1
0	0	1
1	0	X

$S = T$

Q_n \ T	0	1
0	X	0
1	1	0

$R = \overline{T}$

2. Draw the circuit diagram for this :-



SR FF To T FF

SR to JK FF :-

1) Available → SR
   Required → JK

2) Excitation Table → SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3.) characteristic → JK

Q_n	Q_{n+1}	J	K	Q_{n+1}
0	0	0	0	0
0	1	0	1	0
0	0	1	0	1
0	1	1	1	1
1	0	0	0	1
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

4) Boolean expression for SR :-

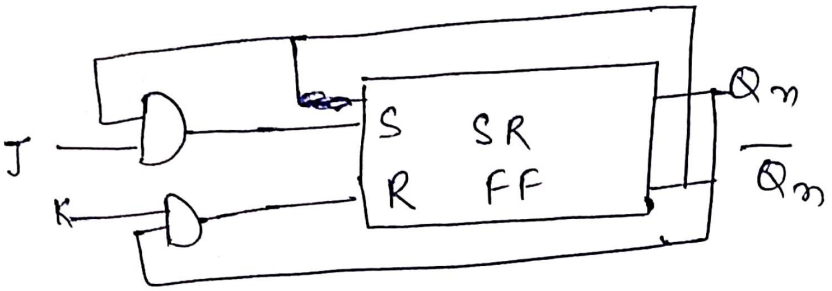
Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	X	0	0	X

$S = \bar{Q}_n J$

Q_n \ JK	00	01	11	10
0	X	X	0	0
1	0	1	1	0

$R = Q_n K$



SR to JK FF